The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte ANDREW MARK NIGHTINGALE and ALISTAIR CRONE BRUCE

Appeal 2007-2701
Application 10/079,811
Technology Center 2100

Decided: September 21, 2007

Before JOSEPH F. RUGGIERO, ANITA PELLMAN GROSS, and ST. JOHN COURTENAY III, *Administrative Patent Judges.*

COURTENAY, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-16. We have jurisdiction under 35 U.S.C. § 6(b). An oral hearing on this appeal was conducted on Sept. 12, 2007.

We REVERSE.

THE INVENTION

The disclosed invention relates to the field of data processing systems. More particularly, the disclosed invention relates to the simulation of data processing systems including both a software component and a hardware component (Specification 2).

Independent claim 1 is illustrative:

1. A method of simulating a system having a software component and a hardware component, said method comprising the steps of:

(i) modelling operation of said software component using a software simulator;

(ii) modelling operation of said hardware component using a hardware simulator;

(iii) linking said hardware simulator and said software simulator to model interaction between said modelled operation of said hardware component and said modelled operation of said software component;

(iv) generating with a test controller, during said modelling of software and hardware components and said interaction, a software stimulus for said software component and a hardware stimulus for said hardware component, said software stimulus and said hardware stimulus are associated so as to permit verification of correct interoperability of said software component and said hardware component, wherein said modelled interaction between said software component and said hardware component proceeds independently of said test controller;

(v) modelling the response of said software component to said software stimulus; and

(vi) modelling the response of said hardware component to said hardware stimulus, wherein said software stimulus is passed to said software simulator by issuing a remote procedure call from said test controller to said software simulator.

THE REFERENCES

Platt	US 5,835,764	Nov. 10, 1998
Hollander	US 6,182,258 B1	Jan. 30, 2001
Campbell	US 6,408,009 B1	Jun. 18, 2002
Harmon	US 6,810,373 B1	Oct. 26, 2004

THE REJECTIONS

Claims 1, 2, 6-12, and 14-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Hollander in view of Platt.

Claims 3-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Hollander in view of Platt, and further in view of Campbell.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Hollander in view of Platt, and further in view of Harmon.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for the respective details thereof.

ISSUE

We find the following issue to be dispositive with respect to all claims on appeal:

Whether the proffered combination of Hollander and Platt teaches and/or suggests recited limitation (i), i.e., "modeling operation of said software component using a software simulator" in combination with the language of limitation (iii) that requires modeling interaction between the modeled operation of the hardware component and the modeled operation of the software component (*see* independent claim 1; *see also* the equivalent language recited in clauses (i) and (iii) of independent claims 15 and 16). *See* Analysis *infra*.

STATEMENT OF LAW

"What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under *§ 103*." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742, 82 USPQ2d 1385, 1397 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 1740, 82 USPQ2d at 1396.

ANALYSIS

We consider the Examiner's rejection of independent claims 1, 15, and 16 as being unpatentable over the teachings of Hollander in view of Platt.

Appellants argue, *inter alia*, that the Examiner has failed to respond to Appellants' argument that limitation (i) of each independent claim is not taught by Hollander or the cited prior art of record (Br. 10, 11, and 17).

Appellants note the Examiner relies upon Hollander at column 8, lines 39-44 and column 10, lines 51-58 for the alleged teaching of "modeling operation of said software component using a software simulator" (independent claim 1; *see also* the equivalent language recited in clause (i) of independent claims 15 and 16). Appellants argue the cited column 8 discussion merely relates to "[a] report generator module 24 [which] provides textual and graphical information on the test results" (Hollander, col. 8, ll. 39-40). Appellants note that the cited column 10 discussion deals with a "co-verification extension module 174" (Hollander, col. 10, ll. 51-52). Appellants conclude that the Examiner has failed to establish a prima facie case of obviousness because at least the limitation of modeling the operation of a software component using a software simulator is not fairly taught or suggested by the proffered combination of Hollander and Platt (Br. 10-11).

The Examiner disagrees. The Examiner notes that Hollander teaches a co-verification module that allows the simultaneous verification of a software component and hardware component (*see* Hollander, col. 10, ll. 51-58). The Examiner finds these two components make up the device-under-test (DUT). The Examiner further notes that Hollander discloses the DUT can be a complete system that comprises hardware having embedded logic (*see* col. 6, lines 50-55). Thus, the Examiner finds the claimed "hardware component" encompasses the hardware portion of Hollander's DUT and the claimed "software component" encompasses Hollander's embedded logic in the DUT (*see* claims 1, 15, and 16). The Examiner points to Hollander's Figure 1 that shows the entire DUT 38 is simulated by Simulator 38. The Examiner contends that in order to simulate the entire DUT, Hollander's

system must be able to simulate the individual modeled software and hardware components of the DUT. The Examiner finds that to perform co-verification, Hollander creates a hardware model where the external software (which is not actual code as alleged by the Appellants, but is the modeled embedded logic of the DUT) is run on the hardware model. Thus, the Examiner concludes that Hollander teaches modeled hardware and software components are simulated (Answer 9).

In the Reply Brief, Appellants contend that the Examiner misunderstands Hollander. Appellants argue that the simulation of the DUT *as a unit* is not necessarily the same as the simulation of *individual software and hardware components* and their *interactions* in order to identify problem sources and causes (Reply Br. 1). Appellants point out that the only structure being tested in Hollander's Fig. 1 is the single DUT 38. Thus, Appellants conclude that Hollander does not teach modeling and testing *individual components* and their *interoperability* (Reply Br. 2, ¶3).

After carefully considering the record before us, we find the weight of the evidence supports the Appellants' position. We begin our analysis by noting that Hollander provides a method and apparatus for functionally verifying an integrated circuit design (i.e., a device under test or DUT)(col. 4, ll. 44-45; *see also* col. 6, ll. 12-15). While Hollander does verify systems that may include embedded software (col. 4, l. 49), we nevertheless find the thrust of Hollander's test generation system is directed to using various Hardware Description Languages (HDLs) to construct and customize verification tests as necessary to "simulate and observe a model of a hardware device." (col. 4, ll. 58-62).

More particularly, we agree with Appellants that Hollander does not teach or fairly suggest modeling software per se. Instead, we find Hollander teaches creating a cyclic-accurate *model of the hardware* on which the external software program runs (col. 10, ll. 24-27). We acknowledge that Hollander's test generation facilities may provide direct inputs to the DUT, as well as inputs to external software (col. 10, ll. 59-61). However, we find that providing inputs to external software for debugging and comparison purposes (col. 11, ll. 2-5) is not the same as modeling operation of the software component using a *software simulator*, such that *interaction is modeled* between the modeled operation of the hardware component and the modeled operation of the software component, as required by the language of each independent claim (claims 1, 15, and 16).

In particular, we find nothing in the record to support the Examiner's contention that Hollander's "external software" is not actual code (as alleged by the Appellants), but is instead the modeled embedded logic of the DUT (*see* Answer 9). Indeed, Hollander expressly discloses an embodiment where the external software is "a driver package [that] can interact with the DUT on one side, as directed by calls to the driver package[']s application programming interface (API) on another side." (col. 12, ll. 11-15). After carefully reviewing the secondary Platt, Campbell, and Harmon references, we find nothing in these references that remedies the deficiencies of Hollander.

For at least the aforementioned reasons, we agree with Appellants that the Examiner has failed to meet the burden of presenting a prima facie case of obviousness. Accordingly, we will reverse the Examiner's rejection of

independent claims 1, 15, and 16 as being unpatentable over Hollander in view of Platt. Because we have reversed the Examiner's rejection of each independent claim, we will not sustain the Examiner's rejection of any dependent claims under appeal. Therefore, we also reverse the Examiner's rejection of dependent claims 2, 6-12, and 14 as being unpatentable over Hollander in view of Platt. Likewise, we reverse the Examiner's rejection of dependent claims 3-5 as being unpatentable over Hollander in view of Platt and Campbell, and we reverse the Examiner's rejection of dependent claim 13 as being unpatentable over Hollander in view of Platt and Harmon.

DECISION

In summary, we will not sustain the Examiner's rejection of any claims under appeal. Therefore, the decision of the Examiner rejecting claims 1-16 is reversed.

REVERSED

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NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203